PATENT ABSTRACTS OF JAPAN

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(54) CACHE MEMORY SYSTEM AND MICROPROCESSOR

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a cache memory control technology for improving through- put by reducing any unnecessary data transfer between a main memory and a cache memory, and reducing power consumption accompanying the data transfer, and relaxing the congestion of paths of the data transfer.

SOLUTION: This cache memory system in which a main CPU is connected with a main memory constituted of an ROM and an RAM through an external bus is constituted of 4-way set associative caches where each Way has Tag 45, Valid bit 46, Dirty bit 47, and data block 48. At the time of driving cache entry out of the cache, when the Dirty bit 47 is set as 1, the data of the data block 48 are written in the main memory, and when the Dirty bit 47 is cleared as 0, the data of the data block 48 are not written in the main memory but discarded.
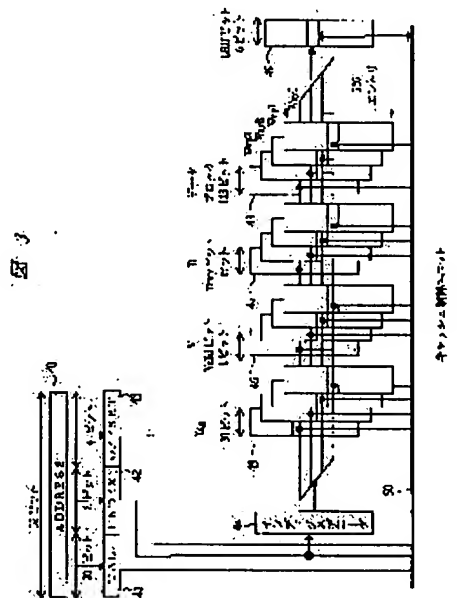
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